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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,501	09/22/2004	Glenn G. Daves	FIS920040002US1	5500

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EXAMINER
ABOAGYE, MICHAEL

ART UNIT	PAPER NUMBER
1725	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,501	DAVES ET AL.	
	Examiner	Art Unit	
	Michael Aboagye	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-12, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. (US Patent No. 6,333,563) in view of Kobayashi (US Patent No. 6,806,560).

Jackson et al. teaches method and an assembling an electronic module comprising: attaching a chip ("10", figure 4) to a substrate ("20", figure 4) using a first solder interconnection array "12", figure 4); attaching a board ("40", figure 4) to said substrate using a second solder interconnection array ("32", figure 4) such that a space

is defined between said board and said substrate, said second solder interconnection array residing entirely within said space (see figure 4); and providing a creep resistant structure or an underfill material within a space between the substrate and the chip, said creep resistant structure being in direct contact with at least said chip and said (column 4, lines 41-58);wherein said creep resistant structure comprising at least one mechanical support structure selected from the group consisting of a bracket, a frame and a collar (note, the examiner interprets the solid copper ball or column recited in column 4, lines 40-50 as being a mechanical support); a single melt (column 3, lines 8-10) and dual melt (column 3, lines 24-27) solder interconnect array, prior to the deposition of the underfill material cleaning the substrate and the circuit board.

Regarding claim 5, Jackson, teaches that the size of the solder ball forming the solder interconnect array is about 508 microns and above (column 3, lines 15) which implies that the gap height residing between the board and the substrate falls within the range from about 300 micron to about 900 microns.

Jackson et al. does not expressly teach providing an underfill material in the space between the circuit board and the substrate and the cleaning step.

However Kobayashi discloses a process for fabricating a surface-mount electronic device wherein an underfill material (“32”, figure 2D) is injected into the clearance i.e. the space between the chip mounting substrate and the printed circuit board (“30”, figure 2D) to enhance the adhesive strength between the chip-mounting substrate and the printed circuit board (abstract, figures 1 and 2D), said under fill material capable of adsorbing the stresses due to thermal expansion coefficient

between the chip –mounting substrate and the printed circuit board and securing the reliability of the soldered joint (Kobayashi, column 1, lines 34-41).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to have modified the method of Jackson et al. by depositing further an underfill material in the space between the circuit board, since the under fill material is capable of adsorbing the stresses due to thermal expansion coefficient between the chip–mounting substrate and the printed circuit board thereby securing the soldered joint and further enhance the adhesive strength between the chip-mounting substrate and the printed circuit board (Kobayashi: abstract, and column 1, lines 34-41).

4. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. (US Patent No. 6,333,563) in view of Kobayashi (US Patent No. 6,806,560) as applied to claim 5 above and further in view of Kumamoto et al. (US Patent No. 6,632,704).

Neither Jackson et al. or Kobayashi expressly teach the properties of the underfill material including density, particles size viscosity dynamic tensile modulus as set forth in claims 14-18.

However, Kumamoto et al., discloses the properties of a desirable epoxy underfill material applied in a surface-mount processing of an electronic devices for the prupose of relieving significant portions of thermal loads induced by coefficient of thermal expansion differences between a chip and a substrate (column 1, line 55- column 2, line 1). Kumamoto et al. teaches an underfill material in its uncured state comprises a

polymeric material having a filler material present in an amount ranging from about 80% by weight per solution said filler material having a particle size ranging from about 4μ - 12μ wherein said underfill material in its uncured state has a density of about 1.8 g/cc, a viscosity at 25.degree. C. greater than about 10,000 cP; wherein said underfill material in its cured state has a glass transition temperature ranging from about 145.degree. C; wherein said substrate comprises a ceramic substrate, said cured underfill material has a CTE below Tg of about 14 ppm/.degree. C and a CTE above the Tg of about 56 ppm/.degree. C (Kumamoto et al. tables 1).

With respect to the tensile strength and the thixotropic index range, though not mentioned by Kumamoto et al., however, the numbers in table 1 of Kumamoto et al., closely match the corresponding numbers describing the properties of the underfill material as set forth in claims 14-18. it is noted that the tensile strength and the thixotropic index range should be about the same considering the fact that said properties are intrinsic.

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to have used the characteristic underfill material of Kumamoto et al. in the method and assembly of Jackson et al. as modified by Kobayashi in order to increase the reliability and the fatigue resistance of the chip substrate interconnection (Kumamoto et al., column 1, lines 59-64).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Vincent (US 6,674,172), Brofman et al. (US 5.968.670) and Sozansky et al. (US 5,953,814) are also cited in PTO-892.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Aboagye whose telephone number is 571-272-8165. The examiner can normally be reached on Mon - Fri 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JONATHAN JOHNSON
PRIMARY EXAMINER

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Michael Aboagye
Assistant Examiner
Art unit 1725
10/06/2006